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Graph-Drawing Contest Report

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Abstract

This report describes the Second Annual Graph Drawing Contest, held in conjunction with the 1995 Graph Drawing Symposium in Passau, Germany. The purpose of the contest is to both monitor and challenge the current state of the art in graph-drawing technology.

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1 Introduction

Text descriptions of three attributed graphs and the contest rules were made available on the World-Wide Web (at http://www.uni-passau.de/agenda/gd95/competition.html and http://www.cs.brown.edu/calendar/gd95/) for this year's contest. The graph attributes included both a *name* and *type* attribute for each vertex. An effective graph drawing had to communicate not only the edge connections between vertices, but also the vertex-attribute values. Thus the main judging criterion was one of information visualization. A secondary criterion was the degree to which the drawing was generated automatically, that is, without manual intervention.

Approximately 40 graphs were submitted by the contest deadline. The emphasis on information visualization and the nature of the graphs resulted in a very eclectic mix of drawings. The winners were selected by a panel of judges, and are shown below.

2 Winning submissions and honorable mentions

2.1 Graph A

Graph A models the architecture of a computer chip and was based on the hand-drawn original shown in Figure 1 [1]. The winning drawing was submitted by Georg Sander of Universität des Saarlandes (sander@cs.uni-sb.de), and is shown in Figure 2. The manual steps needed to produce this drawing included a partitioning of the graph into subgraphs, adjustment of the level assignments of the nodes, and selection of various rendering parameters. Layout was computed automatically using the author's VCG tool in four seconds on a Sparc ELC workstation.

Two other drawings of Graph A received honorable mention. Figure 3 contains the drawing of Paulis Kikusts (paulis@cclu.lv) and Pēteris Ručevskis (rpeteris@cclu.lv) from the University of Latvia. The drawing in Figure 4 was submitted by Thomas Kamps, Jörg Kleinz, and Thomas Reichenberger ([kamps, kleinz, reichen]@darmstadt.gmd.de) from IPSI, GMD Darmstadt.

2.2 Graph B

Graph B represents a collection of global symbols (e.g., functions, types, files, etc.) for a small part of a large X program. The name and type attribute values for this graph's vertices are particularly unwieldy.

The winning drawing for Graph B, shown in Figure 5, was submitted by Falk Schreiber and Carsten Friedrich ([schreibe, friedric]@fmi.uni-passau.de) of Universität Passau. Their strategies for coping with the awkward types and names included the use of color to convey vertex-type information, rotation of the drawing prior to text-label placement to avoid excessive label overlaps, rendering the edges in grayscale to enable visible overprinting

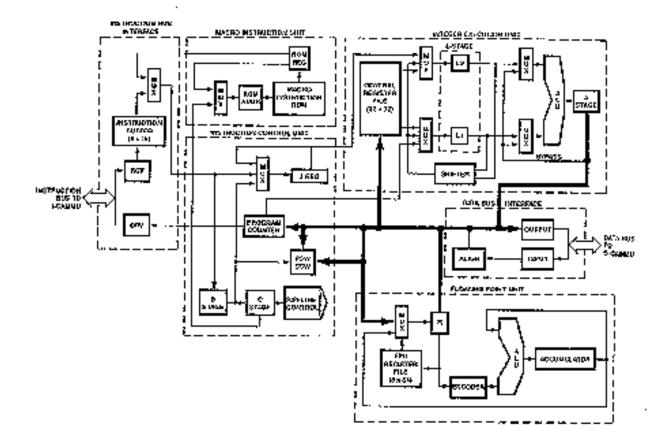


Figure 1: Original hand-drawn copy of Graph A.

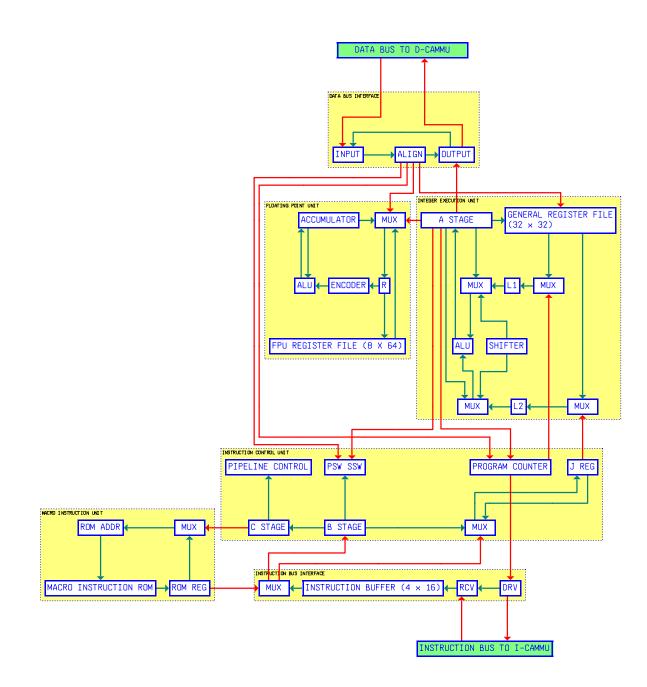


Figure 2: Winner, Graph A.

MUX INTEGER EXECUTION UNIT A STAGE INTEGER EXECUTION UNIT ALU INTEGER EXECUTION UNIT DATA BUS TO D CAMMU EXTERNAL SHIFTER INTEGER EXECUTION UNIT MUX INTEGER EXECUTION UNIT OUTPUT DATA BUS INTERFACE INPUT DATA BUS INTERFACE LI INTEGER EXECUTION UNIT L2 INTEGER EXECUTION UNIT R FLOATING POINT UNIT MUX FLOATING POINT UNIT PROGRAM COUNTER INSTRUCTION CONTROL UNIT ALIGN DATA BUS INTERFACE FPU REGISTER FILE 8 X 64 FLOATING POINT UNIT DRV INSTRUCTION BUS INTERFACE ENCODER MUX INTEGER EXECUTION UNIT INSTRUCTION BUS TO I CAMMU EXTERNAL GENERAL REGISTER FILE 32 X 32 INTEGER EXECUTION UNIT ALU FLOATING POINT UNIT ACCUMULATOR FLOATING POINT UNIT RCV INSTRUCTION BUS INTERFACE MUX INTEGER EXECUTION UNIT J REG INSTRUCTION CONTROL UNIT PSW SSW INSTRUCTION CONTROL UNIT MUX INSTRUCTION CONTROL UNIT PIPELINE CONTROL INSTRUCTION CONTROL UNIT B STAGE INSTRUCTION CONTROL UNIT C STAGE INSTRUCTION CONTROL UNIT Fully automatic pre-layout as ER diagram followed by manual editing of node placement in AUTOMATIC-RECTILINEAR mode automatically avoiding MUX MACRO INSTRUCTION UNIT INSTRUCTION BUFFER 4 X 16 INSTRUCTION BUS INTERFACE MUX INSTRUCTION BUS INTERFACE drawing tool: GRADE Windows (see GD '95 demo) Drawing of graph A by Paulis KIKUSTS and Peteris RUCEVSKIS ROM REG MACRO INSTRUCTION UNIT e-mail: paulis@cclu.lv, rpeteris@cclu.lv ROM ADDR MACRO INSTRUCTION UNIT MACRO INSTRUCTION ROM MACRO INSTRUCTION UNIT node overlapping.

Figure 3: Honorable mention, Graph A.

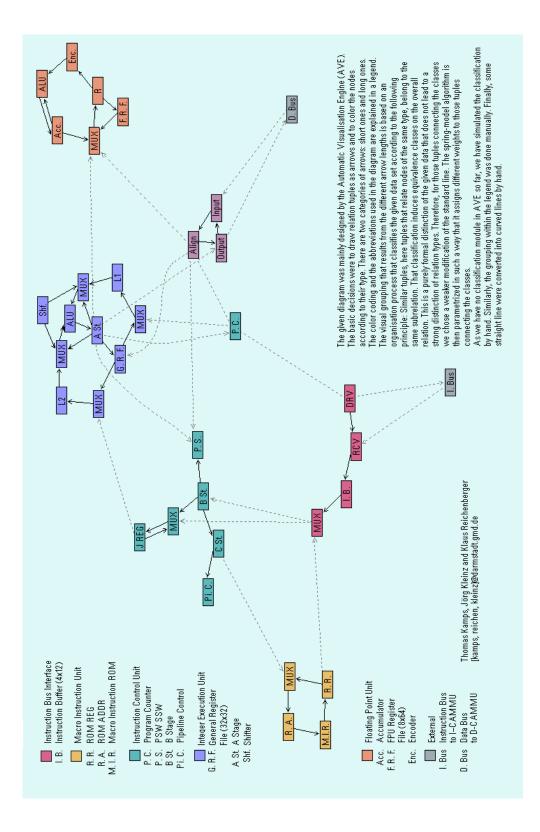


Figure 4: Honorable mention, Graph A.

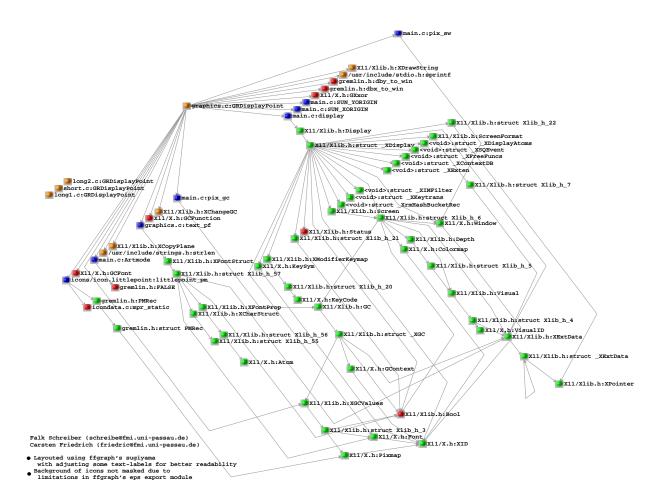


Figure 5: Winner, Graph B.

of text labels, and some manual adjustment of label placements. Layout was performed using a Sugiyama-style algorithm.

Honorable mentions for Graph B went to Georg Sander of Universität des Saarlandes (sander@cs.uni-sb.de) for the drawing in Figure 6 and to Vladimir Batagelj and Andrej Mrvar ([vladimir.batagelj, andrej.mrvar]@uni-lj.si) from the University of Ljubljana for the drawing in Figure 7. In the latter drawing, the text-label problem was finessed by using a legend (not shown) to decode a coloring and numbering of nodes.

2.3 Graph C

Unlike Graphs A and B, Graph C was contrived without reference to a real-world application. However, what it lacks in verisimilitude it makes up for in difficulty, because it is a planar graph that is especially hard to draw well.

Two joint winners were declared for Graph C. They are shown in Figures 8 and 9. The former drawing was submitted by Vladimir Batagelj and Andrej Mrvar ([vladimir.batagelj, andrej.mrvar]@uni-lj.si)from the University of Ljubljana. They used an energy-minimization approach to compute the layout, and manual editing to reposition some nodes. The other winner was submitted by Paulis Ķikusts (paulis@cclu.lv) and Pēteris Ručevskis (rpeteris@cclu.lv) from the University of Latvia. Their approach to layout uses a blend of local placement heuristics, supplemented by some manual editing.

An honorable mention for Graph C was awarded to the entry submitted by Harald Lauer (lauer@informatik.uni-tuebingen) of Universität Tübingen. It is shown in Figure 10.

3 Acknowledgments

Sponsorship for this contest was provided by AT&T Bell Labs, Mitsubishi Electric Research Labs, Tom Sawyer Software, Universität Passau, and Volksbank Passau. Stephen North, Yanni Tollis, and Sue Whitesides assisted with the judging. Stephen North also provided the data for Graph B.

References

[1] W. Hollingsworth, H. Sachs, and A. Smith. The CLIPPER processor: Instruction set architecture and implementation. *CACM*, 32(2):212, February 1989.

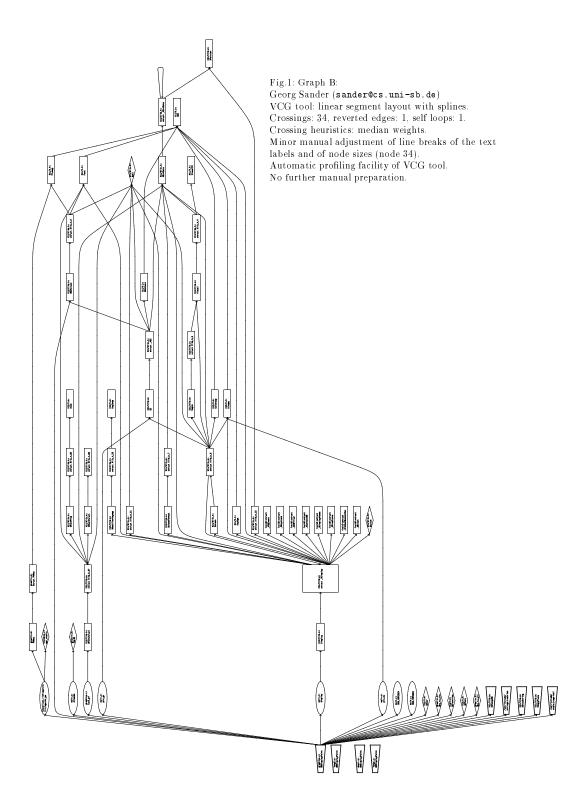


Figure 6: Honorable mention, Graph B.

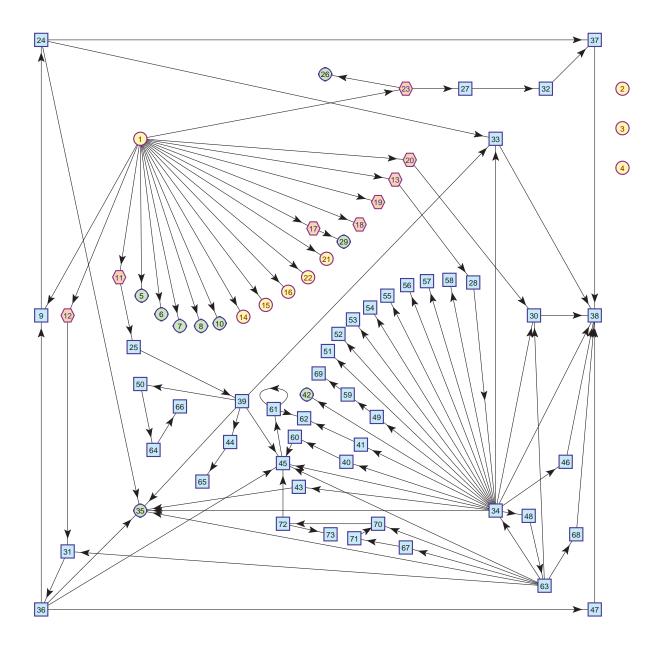


Figure 7: Honorable mention, Graph B.

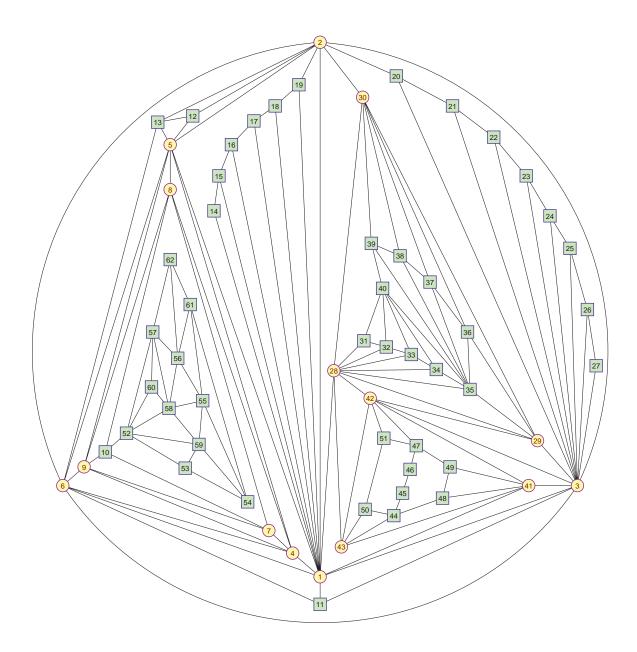


Figure 8: Joint winner, Graph C.

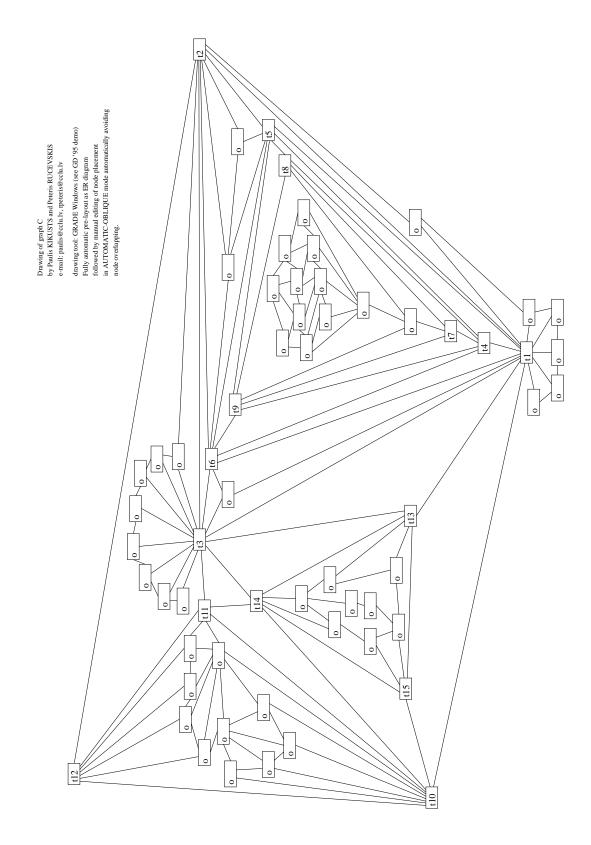


Figure 9: Joint winner, Graph C.

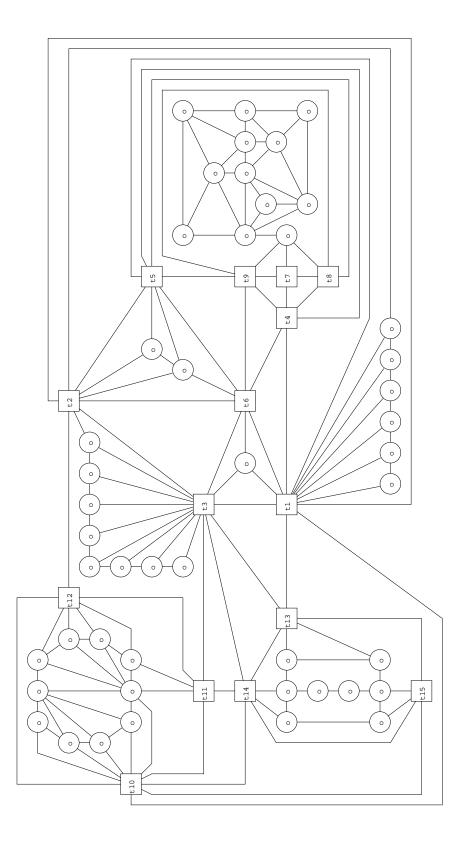


Figure 10: Honorable mention, Graph C.

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