I. INTRODUCTION

To support agile radio operation, software-defined radios (SDR) are investigated to push digital domain further towards antenna. Accordingly, an RF power digital-to-analog converter (DAC) which generates RF signals directly from digital front end is desired to reduce the counts of analog components such as mixers and local oscillators [1].

Recently, Riemann pump (RP) was proposed as a new type of RF-power DAC [1]–[6]. Connected with a power amplifier (PA) directly, it can synthesize nearly arbitrarily RF waveform directly controlled by the output of the PA. The current sources are controlled by switches, according to the desired voltage slope. Since the voltage is expressed as \( v_{out} = \frac{1}{C_{out}} \int_{0}^{t} i_{out}(\tau) d\tau \), the RP can thus control the voltage slope by switching different current sources. The resolution of voltage slope depends on the number of stages of the current sources and current capabilities. In principle, the RP can generate high speed arbitrary RF waveform directly controlled by the output of DSP as shown in Fig. 1, manifesting itself a suitable power DAC for applications of SDR [2]–[6].

II. RIEMANN PUMP (RP) BASICS

Fig. 1 shows the concept of the RP power DAC [2], which is based on binary-weighted current sources that pump charges to input capacitance of the PA. The current sources are controlled by switches, according to the desired voltage slope. Since the voltage is expressed as \( v_{out} = \frac{1}{C_{out}} \int_{0}^{t} i_{out}(\tau) d\tau \), the RP can thus control the voltage slope by switching different current sources. The resolution of voltage slope depends on the number of stages of the current sources and current capabilities. In principle, the RP can generate high speed arbitrary RF waveform directly controlled by the output of DSP as shown in Fig. 1, manifesting itself a suitable power DAC for applications of SDR [2]–[6].

III. PROPOSED ENCODING PATTERNS FOR IMPROVED RP

Conventionally, the high-side and low-side transistors are operated complementary in CMOS process. For example, a 3-stage RP in Fig. 1 has a 3-bit resolution to realize \( 2^3 \) possible currents, \( i_{out} \in \{\pm 1, \pm 3, \pm 5, \pm 7\} i_0 \) for such CMOS operations (e.g., \( A_H \) and \( A_L \) are complementary ON/OFF). However, this CMOS encoding causes undesired current flowing to GND except the case of \( i_{out} = \pm 7 \), because at least one of high-side and low-side transistors have to be ON at the same time. For instance, to generate \( i_{out} = +5 \), \( A_L \) has to be
ON, in addition to $B_H$ and $C_H$ be ON. As a result, it leads to a waste of power, since $i_0$ is following to $A_L$ too. Similarly, this applies for the other power levels as well.

Table I shows our proposed encoding patterns for RP modified for GaN process (considering only the widely available n-channel GaN HEMT device here only, not p-channel), where the high- and low-side transistors are allowed to operate independently. When the input is positive voltage slope, all low-side transistors are turned off, while all high-side ones are OFF for negative voltage slopes. Hence, the current all flows from/to the input capacitance without wasting. It can significantly reduce the driver power consumption. Moreover, since the high-/low-side transistors are controlled independently, the RP bit patterns increased 8 (3-bit) to 15 (3.9-bit) levels compared with the complementary control pattern [1], without increasing the transistor stages as shown in Table I.

### IV. 3-STAGE RF-DAC DESIGN

The signal-to-noise ratio (SNR) in dB is given as follows:

$$\text{SNR}_{\text{dB}} \approx 6.02N + 9.03r - 7.78 + 10 \log \left( 1 - \frac{1}{2^{N-1}} + \frac{1}{2^r} \right)$$

where $N$ is the number of bits, and $r$ is the binary logarithm of the over-sampling ratio (OSR). Specifically, we have OSR = $f_S / f_{\text{max}} = 2^r$ where $f_S$ is the sampling frequency, and $f_{\text{max}}$ is the maximum output frequency. More detail derivations are found in [3]. By comparison with pulse code modulation (PCM) conversion, the SNR of the RP is better than PCM conversion under the condition of $r > 2$ or $r > 1$ and $N > 2$. In this work, we focus on $N = 3.9$ and $r = 2$. For a target fundamental frequency of 2 GHz, $f_S > 16\text{GSa/s}$ is required (OSR = 4). Hence, an SNR of 33 dB is expected from (1).

We designed the 3-stage RF power DAC based on RP architecture shown in Fig. 1. The designed schematic is depicted in Fig. 2. We designed the core transistor size ratio to be $Q_{AH} : Q_{BH} : Q_{CH} : Q_{AL} : Q_{BL} : Q_{CL} = 1 : 2 : 4$, and output capacitor $C_{\text{out}}$ is assumed 20 pF which is equivalent to the input impedance of the PA in [3]. The use of GaN technology restricts the inverter driver to non-complementary transistors, since p-channel GaN HEMT is not widely available. For the digital switching of the GaN power transistors, a switch-mode monolithic microwave-integrated circuit (MMIC) is used, having an implemented DTDR (depletion transistor, depletion and resistive load) driver circuit [3]. The DTDR driver consists of an interconnected depletion-mode transistor and resistive load. It enables both decreased static losses in the driver itself and improved switching characteristic, as mentioned in [7].

In multi-stage RP, it is important to match switching time (rising and falling) of each core transistor because its mismatch leads to distortion of the output voltage. To match the switching time of each core transistor, we optimized DTDR driver transistor size ratio to $Q_{AH} : Q_{BH} : Q_{CH} = 1 : 2 : 4$. According to the proposed encoding table in Table I, each transistor is controlled interdependently. Our designed MMIC layout is shown in Fig. 3. Its fabrication in 150 nm GaN HEMT technology ($f_t = 50 \text{GHz}, f_{\text{max}} = 246 \text{GHz}$) is under the process.
Fig. 4. 3-stage RP output voltage waveform (at 16 GSa/s).

Fig. 5. Voltage waveform of the generated CW 2 GHz at 16 GSa/s.

V. PERFORMANCE RESULTS

We performed harmonic-balance, transient and layout simulations with practical devices non-linear large-signal models including parasitic effects. The simulated output voltage waveforms (ideally triangle wave) for constant current source at 16 GSa/s is shown in Fig. 4. It can be seen that the output voltage is controlled by each input bit pattern (±7i0, ±5i0, ±3i0, ±i0), functioning at 16 GSa/s. The simulated voltage waveform of continuous wave (CW) with a frequency of 2 GHz at 16 GSa/s is also shown in Fig. 5, with spectrum in Fig. 6. It can generate the fundamental frequency 2 GHz CW signal at the 16 GSa/s (OSR = 4).

Based on the above results, it was confirmed that the designed RP circuit achieves the target specification in the simulation. The summary of this work in comparison with the previous work [6] is listed in Table II, showing the improved performance in our design for both SNR and speed.

VI. CONCLUSIONS

We designed a new 3-stage RP using the GaN process to validate the advantage over the existing method. The primary simulation results show a promising performance of the proposed design at high sampling rate of 16 GS/s. Therefore, RP based on GaN with enhanced coding schemes can be a viable candidate for the future digital transmitter in 5G and beyond. We will report experimental results of our RP GaN chip designed for fabrication in the near future.

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REFERENCES


