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Abstract

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Beyond Thermal Management: Incorporating p-Diamond Back-barriers and Cap-layers into AlGaN/GaN HEMTs

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***Abstract*—This work explores the use of p-diamond back-barriers and cap-layers to enhance the performance of GaN-based high electron mobility transistors (HEMTs). Diamond can offer a heavily-doped p-type layer, which are complementary to GaN electronics. Self-consistent electro-thermal simulations reveal that the use of p-diamond back-barriers and cap-layers can increase the breakdown voltage of GaN-based HEMTs by four-fold, at the same time that they enhance the 2DEG confinement and reduce short channel effects. These results highlight that p-diamond layers can improve the performance of GaN HEMTs for high-power and high-frequency applications beyond the thermal improvements pursued until now.**

***Index Terms*— GaN HEMTs, p-diamond back-barrier, p-diamond cap layer, power electronics**

I. Introduction

GaN-based transistors and diodes are excellent candidates for high-voltage and high-frequency electronics. In particular, GaN high electron mobility transistors (HEMTs), which utilize a two-dimensional-electron-gas (2DEG) channel, have demonstrated excellent power and frequency performances [1]. High cut-off frequency over 400 GHz [2] and RF output power over 800 W at 2.9 GHz have been demonstrated in GaN HEMTs [3]. However, applications such as radars for traffic controllers, satellites for broadcasting and high-power motors require an even higher power (~kW) at high-frequency (e.g. K-band), which are still challenging for GaN HEMTs.

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TABLE I
MATERIAL PROPERTIES OF MAJOR SEMICONDUCTORS CONSIDERED FOR POWER AND MICROWAVE APPLICATIONS

	Si	GaAs	SiC	GaN	Diamond
E_g (eV)	1.1	1.4	3.3	3.4	5.5
μ_e (cm^2/Vs)	1400	8000	1000	2000	2000-4500
μ_h (cm^2/Vs)	600	400	100	850	3000-4000
E_c (MV/cm)	0.3	0.4	2.5	3.3	10
k_T (W/cmK)	1.3	0.46	4.2	1.3-2	10-20
ε	11.8	12.9	9.7	9	5.5
Baliga's FOM $\varepsilon\mu E_c^2$	1	15	340	1450	24664

E_g: bandgap; μ_e, μ_h: electron and hole mobility; E_c: critical electric field; k_T: thermal conductivity; ε: dielectric constant. μ_e of 2DEG is used for GaN.

A promising method to further improve the performance of GaN-based HEMTs is to incorporate diamond into the HEMT structure. As shown in Table I, diamond has ~3 times higher critical breakdown field (E_c) and ~10 times higher thermal conductivity than GaN, and has the highest Baliga's Figure of Merit (FOM), a key FOM for high-frequency power device performance [4], among all the potential materials listed [5]. In addition, p-type doping is well established in diamond but still challenging in GaN. Boron doping (p-doping) in single-crystal, polycrystalline and nanocrystalline diamond can reach a concentration as high as 10^{18}-10^{21} cm^{-3} [6][7][8] with free hole concentration over 10^{20} cm^{-3} [8][9]. A hole mobility of 300-600 cm^2/Vs has been demonstrated in p-diamond thanks to hopping transport mechanism [6][10]. In contrast, the p-doping in GaN has a maximum hole concentration of 10^{17}-10^{18} cm^{-3} and maximum hole mobility still below 30 cm^2/Vs [11][12].

Recent progress in GaN and diamond growth have made the integration of diamond and GaN devices possible. GaN layers can be epitaxially grown on [13] or wafer-transferred [14][15] to single-crystal [13] or polycrystalline [14][15] diamond substrates grown by chemical vapor deposition (CVD). Deposition of nanocrystalline diamond (NCD) coating has also been enabled to passivate GaN devices [16]. However, almost all current diamond and GaN integration merely focus on thermal management, which cannot take full advantage of the complementary properties of GaN and diamond.

In this work, we propose to incorporate diamond, as an electronic material, into GaN-based power and microwave devices for the first time. p-diamond is proposed to serve as multi-functional back-barriers or cap-layers for GaN HEMTs.

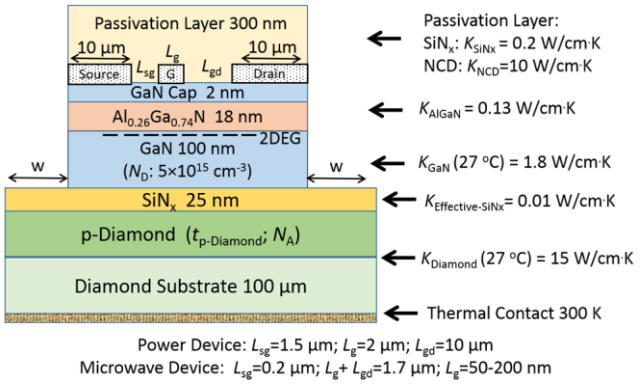

Fig. 1. Schematic structure of a GaN-on-diamond HEMTs with a p-diamond back-barrier. Thermal conductivity of different layers and thermal contact settings are also listed. Two sets of source-to-gate distance (L_{sg}), gate length (L_g) and gate-to-drain distance (L_{gd}) are selected to simulate power and microwave devices.

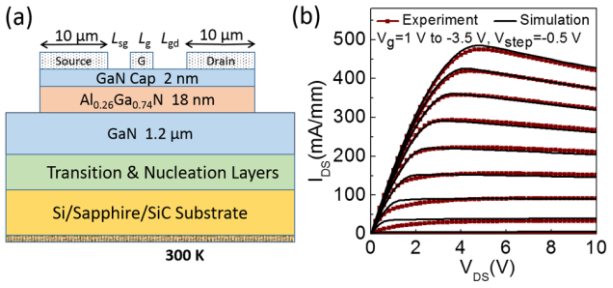

Fig. 2. (a) Schematic of the fabricated AlGaN/GaN HEMT structures on Si/Sapphire/SiC substrates that were used for simulation model calibration. (b) Comparison between simulation and experimental dc output characteristics for a single-finger GaN-on-Si HEMT.

Electro-thermal simulation has demonstrated p-diamond capability in enhancing breakdown voltage, thermal performance and 2DEG confinement for GaN HEMTs. Monolithic and single-finger integration of diamond 2DHG and GaN 2DEG is also proposed for digital and power applications.

II. P-DIAMOND AS A MULTI-FUNCTIONAL BACK-BARRIER

The schematic of the GaN-on-diamond HEMT with a p-diamond back-barrier is shown in Fig. 1. The AlGaN/GaN HEMT layers are based on the GaN-on-Si HEMTs fabricated at MIT [17][18], consisting of 2 nm GaN cap, 18 nm $Al_{0.26}Ga_{0.74}N$ and 100 nm unintentionally-doped GaN (background doping N_D~5×10^{15} cm^{-3}). The 2DEG density was revealed by Hall measurement as 1.25×10^{13} cm^{-2}. The GaN-on-diamond wafer structure is based on the experimental demonstration reported in [14][15], where the GaN layers were extracted from epitaxial GaN-on-Si wafers, followed by the CVD growth of p-diamond back-barrier and 100 μm diamond substrate on top of a ~25 nm intermediate SiN_x dielectric layer. The p-diamond back-barrier thickness and doping concentration are denoted as $t_{p\text{-Diamond}}$ and N_A, respectively. Two sets of source-to-gate distance (L_{sg}), gate length (L_g) and gate-to-drain distance (L_{gd}) are selected to simulate power (Part II B and II C) and microwave devices (Part II D), as shown in Fig. 1.

A. Simulation Model and Calibration

The self-consistent electro-thermal simulations were performed using the Silvaco ATLAS simulator [19], based on the simulation models previously developed for GaN lateral and vertical power devices at MIT [17]. A thermal diffusion region (width w=500 μm) was added for single-finger device simulation and an adiabatic thermal boundary condition was added at the unit-cell sidewall to enable the multi-finger device simulation [17]. The thermal conductivity of different materials in device is listed in Fig. 1. Both NCD (10 W/cm·K [20]) and SiN_x (0.2 W/cm·K) are considered for device passivation. The thermal conductivity of GaN and CVD-grown polycrystalline diamond was set as 1.8 W/cm·K and 15 W/cm·K [14], with a temperature dependence model described in [17]. An effective thermal conductivity of 0.01 W/cm·K for SiN_x transitional dielectrics was calculated from the reported thermal boundary resistance in GaN-on-diamond structures [14]. The diamond bandgap and relative permittivity was set as 5.5 eV and 5.5, respectively; the electron affinity was set as 0.35 eV for a clean reconstructed diamond surface after releasing hydrogen-termination [21] and SiN_x passivation. p-diamond carrier concentration and mobility are based on experimental reports in [8].

The electro-thermal models were calibrated and verified by utilizing the HEMTs structure on Si/sapphire/SiC substrates fabricated at MIT, as shown in Fig. 2 (a). Excellent agreement between experiment and simulation was observed for all devices. A typical comparison between simulation and experimental dc *I-V* characteristics is shown in Fig. 2 (b).

B. Breakdown Voltage Enhancement

The insertion of p-diamond back-barrier can enhance device breakdown voltage (*BV*) by forming a reduced surface field (RESURF) structure. The p-diamond/n-GaN junction below the 2DEG channel can deplete the channel by a vertical electric field (E-field) at off-state, and thus spread the horizontal E-field. As shown in the simulated E-field distribution of GaN HEMTs without and with a p-GaN back-barrier (Fig. 3 (a) and (b)), the p-diamond/n-GaN junction greatly reduces the E-field peak at the gate edge and enables an almost uniform E-field distribution in GaN and diamond between gate and drain. The peak E-field in $Al_{0.26}Ga_{0.74}N$ and GaN was reduced from 15 MV/cm and 8 MV/cm, much higher than the E_c of GaN (3.4 MV/cm) and $Al_{0.26}Ga_{0.74}N$ (5.5 MV/cm for a bandgap of 3.96 eV [22]) , to 4.8 MV/cm and 2.8 MV/cm, at a reverse bias of V_{GS}=-5 V and V_{DS}=1250 V.

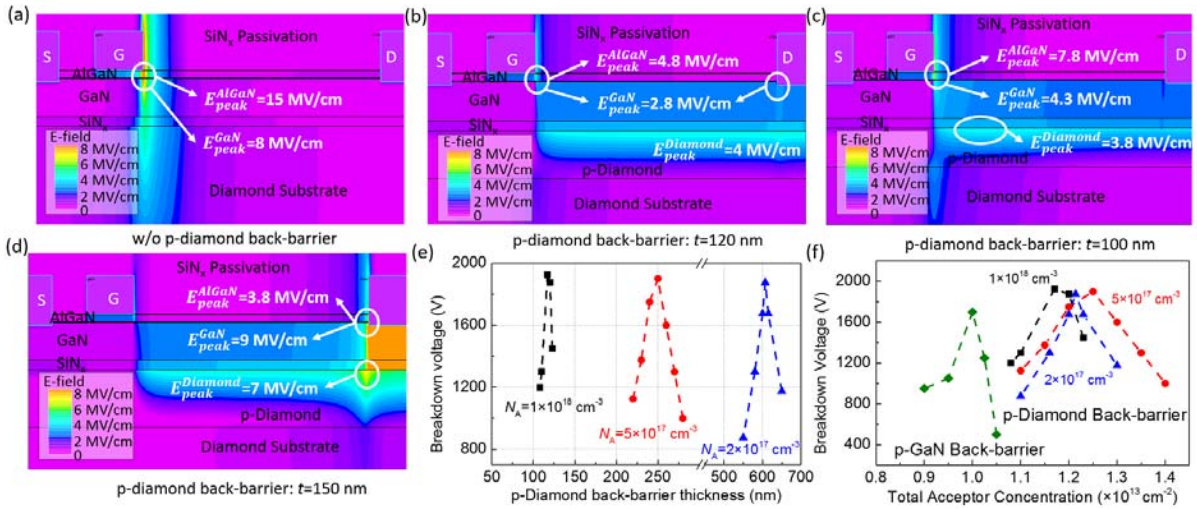

Fig. 3. Simulated electric field distribution in GaN-on-diamond HEMTs (a) without a p-diamond back-barrier and with a (b) 120 nm-, (c) 100 nm- and (d) 150 nm-thick p-diamond back-barrier, all at an off-state bias of V_{GS}=-5 V and V_{DS}=1250 V. The locations of peak E-field in main regions are denoted. (e) Breakdown voltage dependence on p-diamond back-barrier thickness at three different p-diamond doping levels. (f) Breakdown voltage dependence on total acceptor concentration for p-GaN and p-diamond back-barrier.

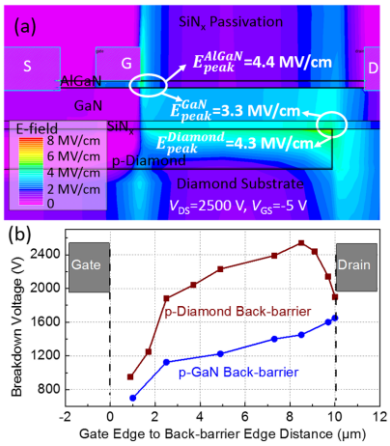

Fig. 4. (a) Simulated electric field distribution in GaN-on-diamond HEMTs with a patterned p-diamond back-barrier, at the bias of V_{GS}=-5 V and V_{DS}=2500 V. The gate edge to back-barrier edge distance is 8.5 μm. (b) Dependence of device breakdown voltage on the gate edge to back-barrier edge distance for GaN HEMTs with p-diamond and p-GaN back-barriers. The geometry and doping of p-GaN and p-diamond back-barrier are extracted from Fig. 3 (f) for a charge balance condition with 2DEG.

The RESURF design principle for HEMTs is to completely deplete the 2DEG charge by the p-n junction at breakdown [23]. In the optimized design, two equal E-field peaks would appear at the gate and drain edge [24], as shown in Fig. 3 (b). In case of charge unbalance, if p-diamond charges are not enough to deplete 2DEG, then a higher E-field peak would appear at the gate edge (Fig. 3(c)); if p-diamond charges are more than 2DEG, then the p-n junction would induce a higher E-field peak at the drain edge (Fig. 3(d)).

In simulation, device BV was extracted when the peak E-field in any region reaches the E_c of corresponding material [17]. The E_c of GaN, $Al_{0.26}Ga_{0.74}N$, diamond and SiN_x were set as 3.4 MV/cm, 5.5 MV/cm, 7 MV/cm (reported for CVD polycrystalline diamond [25]) and 10 MV/cm, respectively. As shown in Fig. 3 (e), a maximum BV of ~1.9 kV can be achieved

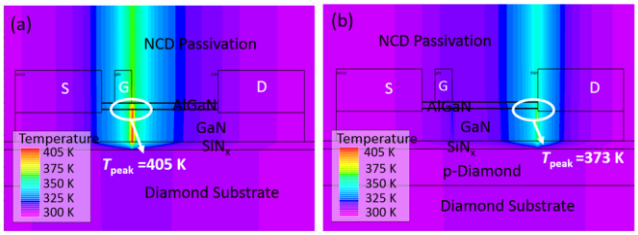

Fig. 5. Simulated lattice temperature distribution in GaN-on-diamond HEMTs (a) without and (b) with a p-diamond back-barrier, at an on-state bias of V_{GS}=0 V and V_{DS}=30 V. The peak temperature and its location are denoted.

by different p-diamond doping concentration N_A, with different optimized p-diamond back-barrier thickness t correspondingly. As shown in Fig. 3 (f), all these optimized N_A and t correspond to the similar total charge density ($N_A \cdot t$) equivalent to the 2DEG density, showing the strong charge balance effect aforementioned. The maximum ~1.9 kV BV is larger than the ~500 V and ~1.65 kV BV of GaN HEMTs without back-barrier and with a p-GaN back-barrier (all with L_{gd}=10 μm), demonstrating the effectiveness of p-diamond back-barrier in BV enhancement.

Under perfect charge balance, a patterned p-diamond back-barrier can further reduce the peak E-field at the drain edge, with the back-barrier edge sitting between gate and drain. Fig. 4 (a) shows the E-field distribution in a HEMT with a patterned p-diamond back-barrier, where the edge of back-barrier is 1.5 μm away from the drain edge horizontally. From the comparison of Fig. 4 (a) and Fig. 3 (b), it can be seen that the patterned p-diamond back-barrier moves the peak E-field location in GaN from the drain edge to the p-diamond/n-GaN junction, creating a more spread E-field distribution in GaN and therefore enabling a higher BV of over 2500 V for L_{gd}=10 μm. The dependence of BV on the patterned p-diamond back-barrier length is shown in Fig. 4 (b), revealing an optimized length L_{BB}^{opt} for maximum BV. The breakdown will occur at the gate edge when the back-barrier length $L_{BB} < L_{BB}^{opt}$,

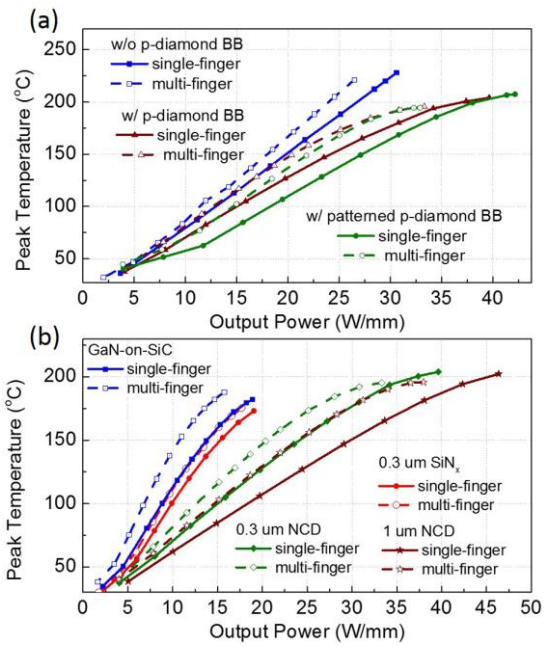

Fig. 6. Simulated peak temperature dependence on output power density for (a) GaN-on-diamond HEMTs with and without a p-diamond back-barrier (BB) and with an optimized patterned p-diamond BB; (b) GaN-on-SiC HEMTs with 0.3 µm SiN_x passivaiton, and GaN-on-diamond HEMTs with 0.3 µm SiN_x, 0.3 µm NCD and 1 µm NCD passivation. Single-finger and multi-finger simulation for all devices are conducted.

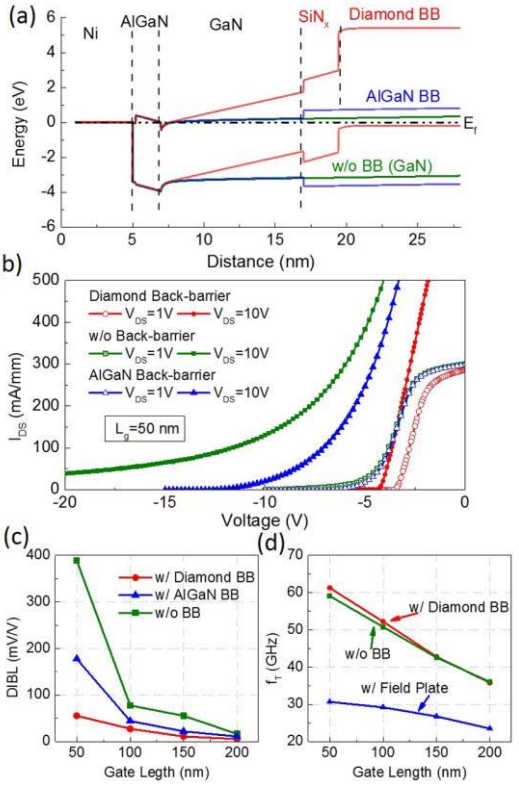

Fig. 7. Simulated (a) band-diagram and (b) transfer characteristics of GaN HEMTs without back-barrier (BB), with a p-diamond BB and with a AlGaN BB. (c) calculated DIBL of the three devices for the gate length of 50, 100, 150 and 200 nm. (d) simulated peak f_T of GaN-on-diamond HEMTs with and without p-diamond BB and with an optimized field plate structure. The AC simulation was conducted at f=1 MHz. All the device simulated in this section utilized L_{sg}, L_g and L_{gd} of the "microwave device" illustrated in Fig. 1.

and at drain edge if $L_{BB} > L_{BB}^{opt}$. This E-field modulation effect was not observed for p-GaN back-barrier, where the peak E-field in GaN always stays near the 2DEG channel rather than moves towards p-n junction and the BV reaches maximum when back-barrier extends to the drain side (Fig. 4 (b)). This is probably due to the relatively small vertical E-field in GaN p-n junctions compared to that in the p-diamond/n-GaN junction.

It should be also noted that the introduction of p-diamond back-barrier does not deteriorate the device forward characteristics. Simulations have revealed only a ~5% on-resistance increase due to the partial depletion of 2DEG by p-diamond back-barrier at on-state. For patterned p-diamond back-barriers with different lengths (Fig. 4), the on-resistance difference is within ~3% from the simulation.

C. *Thermal Performance Enhancement*

In practical applications, the device peak temperature, T_{peak}, is limited to, for example 150 ºC or 200 ºC, to ensure long-term reliable operation. This peak temperature limit determines the device maximumm allowable power dissipation [17]. Thus, power~T_{peak} dependence was simulated to present and compare device thermal performance.

From the simulated lattice temperature distribution shown in Fig. 5, it can seen that the T_{peak} locates at the gate edge in GaN HEMTs without a p-diamond back-barrier and at the drain edge in GaN HEMTs with a p-diamond back-barrier, as a result of the combination of high E-field and high current density [17] at each location. In addition, a lower T_{peak} is observed in GaN HEMTs with a p-diamond back-barrier at the same bias, due to the E-field relaxation by p-diamond back-barrier discussed in the last section. A even lower T_{peak} is observed in GaN HEMTs with an optimized patterned p-diamond back-barrier. Fig. 6 (a) shows the power~ T_{peak} dependence for these three devices with the same material structure but different E-field distribution. For T_{peak}=150 ºC, ~23% higher power density can be achieved by the introduction of p-diamond back-barrier and ~35% higher power by the optimized patterned p-diamond back-barrier.

The influence of the layer structure on the thermal performance was also studied. As shown in Fig. 6 (b), the power~T_{peak} performance of the GaN-on-diamond HEMTs with the same p-diamond back-barrier but different passivation layers were simulated and benchmarked with respect to a GaN-on-SiC device (structure shown in Fig. 2 (a)). As shown for T_{peak}=150 ºC, although the thermal conducvity of polycrystalline diamond is almost 4 times the one of SiC, only ~15% higher power density was achieved in GaN-on-diamond than GaN-on-SiC. The relative small thermal improvement is due to the large thermal boundary resistance of the intermediate dielectric layer used between diamond and GaN [14]. This difference could be even smaller if the thermal conductivity of thin p-diamond layers is lower than the one used in the simulations, taken from thick diamond substrates. However, if the surface passivation material changes from 0.3 µm SiN_x to 0.3 µm NCD, a ~50% power density increase can be achieved. If the thickness of NCD passivaiton increases from 0.3 µm to 1 µm, a power density over 30 W/mm, more than two times that

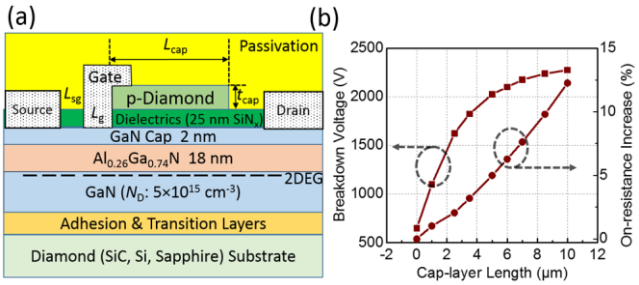

Fig. 8. (a) Schematic structure of the GaN HEMTs with a p-diamond cap-layer. The L_{sg}, L_g and L_{gd} are set as 1.5 μm, 2 μm and 10 μm. (b) Dependence of BV and ΔR_{on} as a function of cap-layer length L_{cap}. The cap-layer thickness t_{cap} and doping level are 60 nm and 1×10^{18} cm^{-3}.

of GaN-on-SiC, can be achieved for T_{peak}=150 °C. These results illustrate the great potential of NCD passivation in the thermal management of GaN power devices.

D. *High-frequency Performance Enhancement*

In GaN-based microwave devices, the gate length is typically scaled down below 200 nm. The short gate length causes short-channel effects such as threshold-voltage (V_{th}) shift, soft pinchoff and high sub-threshold current [26]. A back-barrier structure with high bandgap (e.g. AlGaN [27]) or large polarizaiton charges (e.g. InGaN [26]) has beeen proved as an effective solution for reducing short-channel effects and enhancing 2DEG confinement.

With a larger bandgap than GaN and p-type doping, p-diamond back-barrier can form a large potential barrier that opposes the movement of electrons from 2DEG towards buffer layers, as shown in the simulated band diagram (Fig. 7 (a)). Thanks to the larger energy barrier formed by p-diamond compared to conventional AlGaN back-barrier, short-gate GaN HEMTs with p-diamond back-barirers show not only a much smaller V_{th} shift but also a significant improvement in the subthreshold slope, as shown in Fig. 7 (b). The enhanced suppresion of V_{th} shift by p-diamond back-barrier is more remarkable for shorter gate and higher frequencey devices, as shown in the simulated DIBL (defined as $\Delta V_{th}/\Delta V_{DS}$, and V_{DS} of 1 V and 10 V used in our simulation) as a function of gate length for GaN HEMTs with different back-barriers (Fig. 7 (c)).

Device transfer characteristics were then simulated in ac mode and transconductance g_m, gate capacitances C_{gd} and C_{gs} were extracted as a function of V_{GS}. The intrinsic cut-off frequency f_T was calculated by $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$ for each V_{GS} and the peak f_T was extracted [28]. As shown in Fig. 7 (d), a slight higher f_T is observed in GaN HEMTs with p-diamond back-barriers, indicating the incorporation of p-diamond back-barriers does not diminish device frequency performances. To further compare the BV~f_T trade-off for microwave devices, HEMTs with a gate field plate (FP) are also simulated, as FP is a widely-used method to increase BV. The FP geometry was optimized according to [29]. The FP increases the BV from ~100 V to ~250 V (L_{sg}, L_g and L_{gd} shown in Fig. 1 for 'microwave device'), but introduces additional gate capacitance [29] and greatly reduces the device f_T (Fig. 7 (d)). In contrast, GaN HEMTs with a p-diamond back-barrier, with a ~400 V BV and >60 GHz f_T, outperforms the HEMTs with and without a FP in both BV and f_T.

It should be noted that trapping effects have not been considered in our ac simulation, as negligible current collapse has been reported in GaN HEMTs with either diamond substrates [12] or NCD passivation [13]. In addition, the large potential barrier formed by p-diamond back-barriers would also reduce the possible electron trapping at GaN/SiN_x/diamond interfaces. Thus, we do not expect the trapping effects to significantly diminish the greatly enhanced BV~f_T trade-off in GaN HEMTs with a p-diamond back-barrier. Also, parasitic access resistance and capacitances have not been considered in our simulation. For sub-50nm-gate devices, they need to be considered for accurate device cut-off frequency calculation.

III. P-DIAMOND AS A MULTI-FUNCTIONAL CAP-LAYER

Besides a back-barrier, p-diamond can serve as a multi-functional cap-layer in GaN HEMTs, to enhance BV~R_{on} trade-off and thermal performance (Fig. 8 (a)). P-diamond cap-layer can be grown by CVD on top of dielectric-coated AlGaN/GaN epi-layers [14][15], or possibly deposited by NCD coating [16] following with a p-type doping in NCD [8]. Then the p-diamond can be partially patterned. Gate electrodes form a Schottky contact to the GaN cap layer, and can form either a Schottky or an Ohmic contact (similar to the device in [30] for the Ohmic contact) on the p-diamond cap layer.

Similar to p-diamond back-barrier, p-diamond cap-layer can also compensate 2DEG at off-state to enable a more uniform E-field distribution and a higher BV. Besides total charge amount, a large modulation effect by cap-layer length was also observed for device BV and R_{on}. As shown in Fig. 8 (b), with the p-diamond length extending from gate to drain, a ~3.5 times higher BV can be achieved at the cost of a ~12% higher R_{on}. A great improvement in thermal performance is also seen in GaN HEMTs with p-diamond cap layers, due to relaxed E-field distribution and diamond surface heat spreaders. Similar to results shown in Fig. 6 (b), an additional NCD passivation layer would give best thermal performance. In addition, the p-diamond cap layer, though maybe not so effective in enhancing 2DEG confinement as p-diamond back-barriers, are expected to reduce the electron trapping in AlGaN layer and GaN surface by vertical E-field. This is especially beneficial to GaN high-voltage power devices, as the surface and AlGaN trapping is a critical issue in these devices.

IV. CONCLUSIONS

In this work, we propose new concepts for the integration of p-diamond back-barriers and cap-layers into AlGaN/GaN HEMTs. These new devices take advantage of the complementary electrical properties of diamond and GaN. Electro-thermal simulations have demonstrated a large enhancement in the BV, thermal performance, 2DEG confinement and a reduction of short-channel effects by p-diamond back-barriers or cap-layers. These results show great potential of incorporating p-diamond layers into GaN HEMTs for high-power and high-frequency applications.

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