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A Generalized Admittance Based Method for Fault Location Analysis of Distribution Systems

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***Index Terms*-- Distribution system; equivalent admittance matrix; fault location analysis; short circuit fault**

I. Introduction

With the increasing interests in smart grids, there are growing demands for implementing more advanced applications in distribution automation systems to enable system fault-free or self-healing. Automatic fault location analysis is one of the key applications for achieving fast and accurate fault clearing and service restoration in distribution systems.

Many fault location algorithms have been proposed for distribution systems, including impedance-based methods [1-5], traveling waves based methods [6-9], and knowledge-based approaches [10-11]. Amongst all methods proposed in the literature, impedance-based fault location methods are most generic, practical and straightforward to implement [1, 2]. Unlike traveling waves based methods, no additional equipment, such as the GPS system, fault transient detectors are required for such methods [9]. Also, impedance-based methods require no training sets, thus are more generic in their approach. A two stage fault location algorithm using both pre-fault and fault voltage and current measurements is proposed in [4]. The method makes no assumption regarding the line impedances and load taps, thus it is reasonably accurate even in a heavily taped feeder system. An extended fault-location formulation for a general distribution system is proposed in [5]. The method is based on apparent fault impedance calculation and can calculate sufficiently accurate fault location in a distribution system with intermediate taps, lateral and with heterogeneous lines. Although promising, the impedance-based fault location algorithms developed so far still have few limitations. These algorithms address mostly single-line to ground faults and are applicable to only resistance faults; therefore they result in significant errors in case of impedance fault. Also, these are iterative algorithms and scan the entire distribution feeder to locate the fault, thus doing unnecessary computations.

This paper proposes a novel generalized admittance based method for fault location analysis of distribution systems. The method is proposed based on a realization that for a feeder section, the relationship between the measured currents and voltages at its boundaries can be described using an equivalent admittance matrix that determined by the load demands and topology connections of the feeder section. When a fault occurs, the topology connection of the section will be changed according to the type of the fault, the location of the fault and the fault impedance at the fault location. Therefore, the fault location can be determined by strategically choosing a set of combination of load demands and fault conditions, determining an equivalent admittance matrix for each combination, and finding a correct combination of loads and fault conditions that enables the corresponding equivalent admittance matrix maximally fitting with the relationship between the measured currents and measured voltages. To reduce the computation time, equivalent admittance matrices are determined using different efficient methods according to the measuring ports of the feeder section. The computation is further reduced by dividing the fault location analysis into a set of less computation-intense sub-tasks, including fault type and faulted section determination, faulted section's load demand estimation, fault line segment and fault impedance determination, and fault location determination. Test results on a sample system are given to demonstrate the effectiveness of proposed approach.

II. Fault Type and Faulted Feeder Section Determination of Distribution Systems

A. Distribution Systems with Adanced Protection Scheme

The proposed method is developed for a radial distribution system with advanced protection scheme in which each feeder fed by the transformer in the distribution substation has one feeder breaker located at the substation, and several intelligent switches along the feeder. The breakers and switches are both equipped with sensor units that can provide three-phase voltage and three-phase current measurements.

Based on the location of measurable switches, each feeder can be partitioned into several feeder sections. A feeder section can be categorized as a one-port section, a two-port section, or a multi-port section when there are one, two or multiple measurable devices located at its boundaries, respectively.

Fig. 1 shows an example of distribution systems with advanced protection scheme. In the distribution substation, there are two feeders connected with the transformer downstream, including feeder FDR-I, and feeder FDR-II. Taken feeder FDR-1 as example, it has one feeder breaker, three intelligent switches, and four feeder sections. Among those feeder sections, section-I-1 is a three-port section, section-I-2 is a two-port section, and section-I-3 and section-I-4 are one-port section.

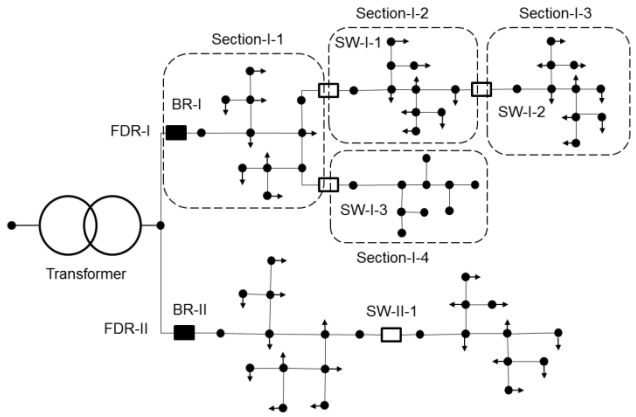

Figure 1. An example of Distribution Systems with Advanced Protection Scheme

For a distribution system without advanced protection scheme, each feeder only has one measurable switch, i.e., feeder breaker. In this case, each feeder can be treated as a one-port section, and the fault location on the feeder can be determined using the method proposed for one-port section in this paper.

B. Determining the Fault Type and Faulted Feeder Section

To reduce the computation burden of fault location determination, the analysis is first narrowed down to a specific type of fault, and a specific section of a feeder.

The fault type and faulted feeder section are determined based on the measured voltages and currents at fundamental frequency on the feeder breakers and intelligent switches taken during the fault. The determination method may be slightly different for a grounded distribution system and an ungrounded distribution system. Due to the space limitation, this paper only provides the method for ungrounded systems.

The fault type is determined based on the status of over-current and over-voltage of a feeder breaker during the fault. If there are no over-currents or over-voltages on any phase of the breaker, then there is no fault downstream to the breaker. If there are no over-currents but over-voltages, the fault is a single-phase-to-ground fault. If there are two phases having over-currents and the phase without over-current having over-voltage, then the fault is s double-phase-to-ground fault. If there are two phases having over-currents but no over-voltage on the phase without over-current, the fault type is phase-to-phase fault. If there are three phases having over-currents, then there is a three-phase-to-ground fault or phase-to-phase-to-phase fault downstream to the feeder breaker.

The faulted feeder and faulted feeder section are determined using different approaches for a single-phase fault, and a non-single phase fault.

For a non-single phase fault, a feeder is determined as a faulty one, if there are over-currents on its breaker. The phases that have over-currents are the faulty phases. A faulted feeder section is the farthest section from the root of feeder that has over-currents on its upstream switch.

For a single-phase-to-ground fault, a feeder is faulty if the phase angle difference between the residual voltage and residual current measured at the feeder breaker are close to 90 degree:

$$\left|\angle V_{fdr}^{res} - \angle I_{fdr}^{res} - 90°\right| < \Delta\bar{\theta} \quad (1)$$

where, $\angle \mathrm{V}_{\mathrm{fdr}}^{\mathrm{res}}$ is the phase angle of residual voltage measured at the feeder breaker, $\angle I_{fdr}^{res}$ is the phase angle of residual current flowing on the feeder breaker, $\Delta\bar{\theta}$ is a threshold for angle difference determination, for example, $\Delta\bar{\theta}$ is set to be 20 degree. A feeder section is determined as faulty when the angle difference between a residual voltage V_{up}^{res} and a residual current I_{up}^{res} at its upstream switch *up* is close to 90 degrees, and the angle difference between residual voltage V_{dn}^{res} and residual current I_{dn}^{res} at one of its downstream switch *dn* (if available) is close to -90 degrees:

$$\left|\angle V_{up}^{res} - \angle I_{up}^{res} - 90°\right| < \Delta\bar{\theta} \quad (2)$$

$$\left|\angle V_{dn}^{res} - \angle I_{dn}^{res} + 90°\right| < \Delta\bar{\theta} \quad (3)$$

Only (3) is used to determine whether there is a fault within the section, if the residual current at the upstream switch is close to be zero.

The residual voltage and current for switch *p* are determined according to:

$$V_p^{res} = \sum_{x\in\{a,b,c\}} V_{p,x} \quad (4)$$

$$I_p^{res} = \sum_{x\in\{a,b,c\}} I_{p,x} \quad (5)$$

where, $V_{p,x}$ is the voltage measured at the switch *p* on phase *x*, and $I_{p,x}$ is the current flowing on the switch *p* of phase *x*.

III. Determining Equivalent Admittance for Faulted Feeder Section

The proposed method treats all loads of the faulted feeder section as constant impedance loads, and assumed that there are no generation resources in the section. Accordingly, for the faulted section, the relationship between measured currents and voltages at its boundaries can be represented as:

$$\mathrm{I}_{\mathrm{port}} = \mathrm{Y}_{\mathrm{eqv}}\mathrm{V}_{\mathrm{port}} \quad (6)$$

where, $\mathrm{I}_{\mathrm{port}}$ is the vector of injected currents for all phases of its measuring ports, $\mathrm{V}_{\mathrm{port}}$ is the vector of terminal voltages for all phases of its measuring ports, and $\mathrm{Y}_{\mathrm{eqv}}$ is an equivalent admittance matrix determined for the section.

The equivalent equivalence matrix is determined by the load demands and topology connections of the feeder section. When a fault occurs, the topology connection of the section will be changed according to the type of the fault, the location of the fault and the fault impedance at the fault location. The proposed method determines the location of the fault by strategically choosing a set of combination of load demands and fault conditions, determining an equivalent admittance matrix for each combination, and finding a correct combination of loads and fault conditions that enables the corresponding equivalent admittance matrix maximally fitting with the relationship between the measured currents and measured voltages as expressed in (6).

To more efficiently determining the equivalent admittance matrix for a feeder section under various load and fault conditions, different solution methods are used

according to the number of its measuring ports. A topology and circuit analysis based method is used for a feeder section with one or two measuring ports, and a Kron reduction based method is used for a feeder section with more than two measuring ports.

A. Determining Equivalent Admittances for One-Port Feeder Sections

For a one-port feeder section, the equivalent admittance matrix can be determined through topology and circuit analysis of its branch connections and admittance models of the branches.

For any branch between an upstream bus p and a downstream bus s, its admittance model can be described as:

$$\begin{bmatrix} I_{ps} \\ I_{sp} \end{bmatrix} = \begin{bmatrix} Y_{ps}^{pp} & Y_{ps}^{ps} \\ Y_{ps}^{sp} & Y_{ps}^{ss} \end{bmatrix} \begin{bmatrix} V_p \\ V_s \end{bmatrix} \quad (7)$$

where, I_{ps} and I_{sp} are the vectors of phase currents flowing from bus *p* to bus *s* , and bus *s* to bus *p* on the branch, V_p and V_s are the vectors of phase voltages at bus *p* and bus *s* respectively. Y_{ps}^{pp} and Y_{ps}^{ss} are the self-admittance matrices at bus *p* and bus *s*, and Y_{ps}^{ps} and Y_{ps}^{sp} are the mutual admittance matrices between bus *p* and bus *s*, and bus *s* and bus *p*, respectively. For any un-faulted branch, a corresponding admittance model can be formulated using (7) according to its branch type.

When a fault occurs at a line segment, (7) can still be used to model the faulted segment by using the method proposed in [12]. For the faulted line segment, its corresponding admittance matrices can be determined by merging its normal admittance matrix with the fault conditions.

The equivalent admittance matrix for the faulted feeder section is determined by sequentially combining one-port equivalent admittance matrices of each line segment or branch determined starting from the farthest buses of the feeder section to the upstream switch of the section.

For each branch between an upstream bus *p*, and a downstream bus *s*, an equivalent one-port admittance matrix Y_{ps}^{1port} for the portion of the feeder section defined by the branch and all devices downstream to the downstream bus *s* is determined based on loads at the downstream bus *s*, and branches connected downstream to bus *s*, according to:

$$Y_{ps}^{1port} = Y_{ps}^{pp} - Y_{ps}^{ps}\left(Y_{ps}^{ss} + Y_{s}^{load} + Y_{s}^{cap} + \sum_{t\in DD_s} Y_{st}^{1port}\right)^{-1} Y_{ps}^{sp} \quad (8)$$

where, Y_{s}^{load} and Y_{s}^{cap} are the equivalent admittance matrices of loads and capacitors connected to bus *s*, Y_{st}^{1port} is the equivalent one-port admittance matrix for the portion of the feeder section defined by the branch between bus *s* and bus *t* and all devices downstream to the bus *t*, DD_s is the set of downstream branches that directly connected with bus *s*.

B. Determining Equivalent Admittances for Two-Port Feeder Sections

The equivalent admittance matrix for a two-port feeder section is determined by sequentially combining two-ports equivalent admittance matrices of each line segment on the mainline determined starting from the downstream port of the faulted section to the upstream port. The mainline refers to the shortest path between two measuring ports.

If any terminal bus of a line segment is connected with a lateral, the corresponding equivalent admittance matrix for the lateral are first determined using method for one-port feeder section, and then merged into the two-port equivalent admittance matrix of the line segment.

For a branch between an upstream bus *p* and a downstream bus *s* on the mainline, a 6-by-6 equivalent admittance matrix, Y_{ps-dn}^{2port} is used to represent the relationship of voltages and injected currents of two-port feeder portion between the branch and the downstream measuring port *dn*. This equivalent admittance matrix includes four 3-by-3 sub-matrices:

$$Y_{ps-dn}^{2port} = \begin{bmatrix} Y_{ps-dn}^{2port,pp} & Y_{ps-dn}^{2port,pd} \\ Y_{ps-dn}^{2port,dp} & Y_{ps-dn}^{2port,dd} \end{bmatrix} \quad (9)$$

where $Y_{ps-dn}^{2port,pp}$ and $Y_{ps-dn}^{2port,dd}$ are the self-admittance matrices for the bus *p* and the downstream measuring port, *dn*. $Y_{ps-dn}^{2port,pd}$ and $Y_{ps-dn}^{2port,dp}$ are the mutual admittance matrices between the bus *p* and the downstream measuring port, and the downstream port and bus *p*. Similarity, for a branch between an upstream bus *s* and downstream bus *t*, we can have:

$$Y_{st-dn}^{2port} = \begin{bmatrix} Y_{st-dn}^{2port,ss} & Y_{st-dn}^{2port,sd} \\ Y_{st}^{2port,ds} & Y_{st-dn}^{2port,dd} \end{bmatrix} \quad (10)$$

where, Y_{st-dn}^{2port} is the two-port equivalent admittance matrix for the portion between the branch of bus *s* and bus *t*, and the downstream measuring port *dn*. $Y_{st-dn}^{2port,ss}$ and $Y_{st-dn}^{2port,dd}$ are the self-admittance matrices for the bus *s* and the downstream measuring port *dn*. $Y_{st-dn}^{2port,sd}$ and $Y_{st}^{2port,ds}$ are the mutual admittance matrices between the bus *s* and the downstream measuring port *dn*, and the downstream measuring port *dn* and the bus s.

The two-port equivalent admittance matrix for the portion of feeder between the branch of bus *p* and bus *s*, and the downstream measuring port *dn* is determined according to:

$$Y_{ps-dn}^{2port,pp} = Y_{ps}^{pp} - Y_{ps}^{ps}\left(Y_{st-dn}^{2port,ss} + Y_{s}^{load} + Y_{s}^{cap} + \sum_{l\in LT_s} Y_{sl}^{1port}\right)^{-1} Y_{ps}^{sp} \quad (11)$$

$$Y_{ps-dn}^{2port,pd} = -Y_{ps}^{ps}\left(Y_{st-dn}^{2port,ss} + Y_{s}^{load} + Y_{s}^{cap} + \sum_{l\in LT_s} Y_{sl}^{1port}\right)^{-1} Y_{st-dn}^{2port,sd} \quad (12)$$

$$Y_{ps-dn}^{2port,dp} = -Y_{st-dn}^{2port,ds}\left(Y_{st-dn}^{2port,ss} + Y_{s}^{load} + Y_{s}^{cap} + \sum_{l\in LT_s} Y_{sl}^{1port}\right)^{-1} Y_{ps}^{sp} \quad (13)$$

$$Y_{ps-dn}^{2port,dd} = Y_{st-dn}^{2port,dd} - Y_{st-dn}^{2port,ds}\left(Y_{st-dn}^{2port,ss} + Y_{s}^{load} + Y_{s}^{cap} + \sum_{l\in LT_s} Y_{sl}^{1port}\right)^{-1} Y_{st-dn}^{2port,sd} \quad (14)$$

where, LT_s is the set of buses on the laterals and connected to the main line bus *s*. Y_{sl}^{1port} is the 1-port equivalent admittance matrix for the lateral downstream to the upstream bus of the branch between an upstream bus *s* and a downstream bus *l*.

C. Determining Equivalent Admittances for Multi-Port Feeder Sections

The equivalent admittance matrix for a feeder section with more than two measuring ports can be determined by applying Kron reduction to an admittance matrix for all buses of the faulted section to remove all elements of the

equivalent admittance matrix corresponding to buses with zero injected currents.

An equivalent admittance matrix for all buses of the section can be first built to express the relationship between injected currents and voltages for all buses in the feeder section:

$$I_{all} = Y_{fll}^{sect} V_{all} \quad (15)$$

where, I_{all} is the vector of injected currents for all phases of each bus in the section, V_{all} is the vector of voltages on all phases of each bus in the section, Y_{full}^{sect} is the full admittance matrix for the feeder section. All loads and capacitors are converted into impedances to be included in the full admittance matrix. Then a Kron reduction is applied to the full admittance matrix to remove all buses with zero injected currents. After the reduction, only the buses at the terminals of measuring ports are left:

$$I_{port} = Y_{eqv}^{mport} V_{port} \quad (16)$$

where, I_{port} is the vector of injected currents for all phases of each measuring port in the section, V_{port} is the vector of voltages on all phases of each measuring port in the section, Y_{eqv}^{mport} is the required multi-port equivalent admittance matrix for the feeder section.

IV. Determining the Load Demands of Fauled Feeder Section

The load demands for the faulted feeder section are unknown, and determined using the pre-fault voltage and current measured at the boundaries of the feeder section and given load profiles for individual loads in the section.

In this paper, each load is approximated as a product of base load given by load profile and a set of uniform load scaling factors determined for all loads in the section. Taken DELTA-connected loads as example, the power consumption of an individual load connected to bus *p* between phase *x* and phase *y*, $S_{p,xy}$ is defined as:

$$S_{p,xy} = \alpha_{xy} S_{p,xy}^{base} \qquad xy \in \{ab, bc, ca\} \quad (17)$$

where $S_{p,xy}^{base}$ is the base power consumption given by load profile for the time interval of fault occurring, and α_{xy} is an uniform scaling factor used for all load components between phase *x* and phase *y* in the feeder section.

The load scaling factors are determined by finding a set of scaling factors with minimal current mismatch between the currents measured at the boundaries of the section, and the estimated currents determined by multiplying the equivalent admittance matrix and measured voltages at the boundaries of the section:

$$\min_{\alpha_{xy}} \{ \left\| I_{meas}^{normal} - I_{est,\alpha_{xy}}^{normal} \right\| \} \quad (18)$$

where, I_{meas}^{normal} is the vector of injected currents of all phases for each measured port determined according to the pre-fault measured currents at the ports, $I_{est,\alpha_{xy}}^{normal}$ is the estimated injected currents determined as:

$$I_{est,\alpha_{xy}}^{normal} = Y_{eqv,\alpha_{xy}}^{normal} V_{meas}^{normal} \quad (19)$$

$Y_{eqv,\alpha_{xy}}^{normal}$ is the normal equivalent admittance for the section determined using loads corresponding to a given set of load scaling factors α_{xy}. V_{meas}^{normal} is the vector of pre-fault measured voltages for all phases of measured ports. $\|.\|$ is an Euclidean distance.

An iterative procedure can be used by adjusting the scaling factors for each phase pair with small increments or decrements, until a minimal distance of normal current mismatches at the boundaries of the section is obtained.

V. Determining the Faulted Line Segment and Fault Location

The faulted line segment is determined as a line segment adjacent to a bus that has minimal fault current mismatches between the measured during-fault currents, and estimated fault currents determined as a product of an equivalent admittance matrix and measured during-fault voltages, and the equivalent admittance matrix is determined by applying determined type of type and a specific set of fault impedances to the bus.

An iterative procedure is used to find a bus in the section and coupled with a specific set of fault impedances that has the minimum distance for fault current mismatches:

$$\min_{p,Z_f} \{ \left\| I_{meas}^{fault} - I_{est,p,Z_f}^{fault} \right\| \} \quad (20)$$

where, I_{meas}^{fault} is the vector of injected currents for all measuring ports determined according to the measured fault currents at the ports, I_{est,p,Z_f}^{fault} is the vector of estimated injected fault currents when the bus *p* has a determined type of fault, and given fault impedance Z_f, and determined according to:

$$I_{est,p,Z_f}^{fault} = Y_{eqv,p,Z_f}^{fault} V_{meas}^{fault} \quad (21)$$

Y_{eqv,p,Z_f}^{fault} is the equivalent admittance matrix for the section determined by applying the determined type of fault and given fault impedance Z_f at the bus *p*. If multiple candidate line segments are found, the actual fault line segment can be found by checking the fault current mismatches at an additional point in the vicinity of the determined bus on each candidate segment, and the candidate with minimal mismatches on the additional point is the faulted line segment. For example, the additional point can be selected as one that is 0.00001 mile from the determined bus.

After the faulted line segment and associated fault impedances are determined, the location of the fault can be determined by finding a location along the determined fault line segment with determined type of fault and fault impedances that has minimal fault current mismatches between the measured fault currents and estimated fault currents:

$$\min_{loc} \left\| I_{meas}^{fault} - I_{est,loc}^{fault} \right\| \quad (22)$$

where, $I_{est,loc}^{fault}$ is the vector of estimated injected fault currents at the boundaries of the section when the determined fault type with determined fault impedances is applied to the location *loc* along the determined line segment, and determined as:

$$I_{est,loc}^{fault} = Y_{eqv,loc}^{fault} V_{meas}^{fault} \quad (23)$$

$Y_{eqv,loc}^{fault}$ is the equivalent admittance matrix for the section determined by applying the determined fault type with determined fault impedances to the location *loc* along the determined line segment.

VI. Numerical Examples

The proposed method has been tested with several sample systems, and satisfactory results are obtained. Fig. 2 gives an example of ungrounded distribution systems.

As shown in Fig. 2, the system includes 1 three-phase

transformer and 3 feeders. Each feeder has 1 feeder breaker, 2 intelligent switches, 18 three-phase three-wire line segments, and 22 three-phase buses. All buses are connected with DELTA-connected constant-PQ loads. Each line segment is a 1.25-mile long underground-cable, and the maximum length for each feeder is 15 miles. The self-impedances of line segments at phase A, B and C are (0.4751+j0.2973), (0.4488+j0.2678), and (0.4751+j0.2973) ohms per mile respectively. The mutual impedances between phases A and B, B and C, and C and A are (0.1629-j0.0326), (0.1629-j0.0326), and (0.1234-j0.0607) ohms per mile. The self-susceptance of each phase is 127.8306 micro Siemens per mile. The tests are conducted with an Intel i5-2.40GHz CPU.

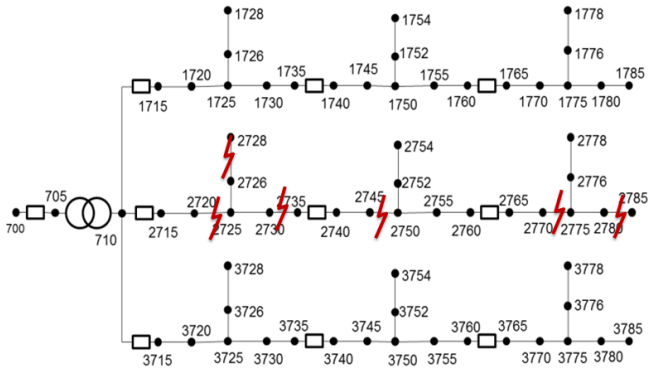

Figure 2. A sample ungrounded distribution system

Due to the space limitation, only the results on two typical fault types are given here. Table I lists the test results on single-phase-to-ground faults, and table II shows the results on phase-to-phase faults. For each type of fault, six different fault locations are tested. The actual fault is located at a location with distance of 47.25% of the line length from the upstream terminal of the line segment. The incremental distance step used is 0.003 miles.

TABLE I. TEST RESULTS ON SINGLE-PHASE-TO-GROUND FAULTS

Fault Location	Prediction Error(miles)	Computation Time(ms)
2720-2725	0.003	87.291
2730-2735	0.003	87.525
2745-2750	0.003	37.562
2726-2728	0.003	81.834
2752-2754	0.003	40.716
2770-2775	0.003	30.135
2780-2785	0.003	30.412

TABLE II. TEST RESULTS ON PHASE-TO-PHASE FAULTS

Fault Location	Prediction Error(miles)	Computation Time(ms)
2720-2725	0.003	107.050
2730-2735	0.003	105.053
2745-2750	0.003	48.400
2726-2728	0.003	106.345
2752-2754	0.003	48.146
2770-2775	0.003	38.483
2780-2785	0.003	39.064

As shown in the tables, the proposed method can generate fault location results with prediction error of 0.003 miles in 107 milliseconds. It should be noted that the prediction accuracy and computation time are heavily depended on the minimum incremental fault distance step. If the incremental distance step is small enough, the proposed approach is capable of producing very accurate fault location results. A good compromise between prediction accuracy and computation time is needed for the real applications of the proposed approach.

VII. CONCLUSIONS

This paper has proposed a novel generalized admittance based method for fault location analysis of distribution systems. It can be used for any type of short-circuit fault, including single-phase-to-ground fault, phase-to-phase fault, double-phase-to-ground fault, three-phase-to-ground fault, and phase-to-phase-to-phase fault. It can also be used for bolted faults, and impedance faults.

An equivalent admittance matrix for the faulted feeder section determined for a given load or fault conditions is used to check whether a candidate set of loads or fault conditions fit with the relationship between measured currents and voltages at the boundaries of the feeder section. The computation time is reduced by determining equivalent admittance matrices using different efficient methods according to the measuring ports of the feeder section.

The computation is further reduced by dividing the fault location analysis into a set of less computation-intense sub-tasks, such as fault type and fault feeder section determination, feeder section load estimation, fault line segment and fault impedance determination, and fault location determination.

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