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TR2014-014 March 2014

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2014 IEEE International Wireless Symposium (IWS)

FPGA Implemented Multi-Level IFPWM Power Coding for Class-S PA in an All-Digital GHz LTE Transmitter

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***Abstract* — This work presents a new efficient multi-level intermediate frequency pulse width modulation (ML-IFPWM) power coding algorithm for switch-mode power amplifier. The merits of high power coding efficiency with distortion correction function are demonstrated by a FPGA implemented digital front end. Measurement results have shown power coding efficiency greater than 45%. To our knowledge, this is the firstly reported implemented discrete-time domain 3-level power encoding approach with 5-MHz LTE signal at RF carrier frequency around 2 GHz. This can be used to generate multi-level digital pulse-train for advanced class-S PA in cellular digital base stations.**

***Index Terms* — Digital-RF transmitter, FPGA, multi-level encoder, power coding efficiency, pulse width modulator (PWM), microwave power amplifiers, switch-mode PA.**

I. INTRODUCTION

With the rapid evolution of modern mobile wireless communications, multi-band and multi-mode (e.g. MC-GSM, WCDMA, LTE, LTE-Advanced) operations are needed at both base station and handset. Consequently, the ever increasing complexities of the radio networks demand further adaptability, agility, as well as intelligence (i.e. cognitive radio) on the radio transmitter (TX), which is one of the most challenging modules in the software-defined-radio (SDR).

To date, All-Digital TX architectures are under intensive research due to its unique advantages such as flexibility, and immunity to the RF analog impairments. RF power amplifier (PA) is the most critical component in the radio front-end. As shown in Fig.1, depending on the operation of power amplifiers, there are basically two kinds of digital-RF TX architecture. One is based on the linear PAs (Si-based), in which the RFDAC or the digital-RF converter (DRFC) buffer the multi-bits data from digital low-pass filters, and then feed to linear PA, popular for low-power handheld terminals; the other consists of normally switch mode power amplifiers (SMPA) like high efficiency class-D or class-S. Here, a particularly important power coding block is necessary to quantize the modulated signal with varying envelope (like OFDM) and thus to generate high speed digital-RF pulse bits for SMPA. In recent years, the advancement of GaN HEMT transistor technologies (higher power density, f_t, and lower switching loss) has made this architecture very attractive for digital base station applications [1].

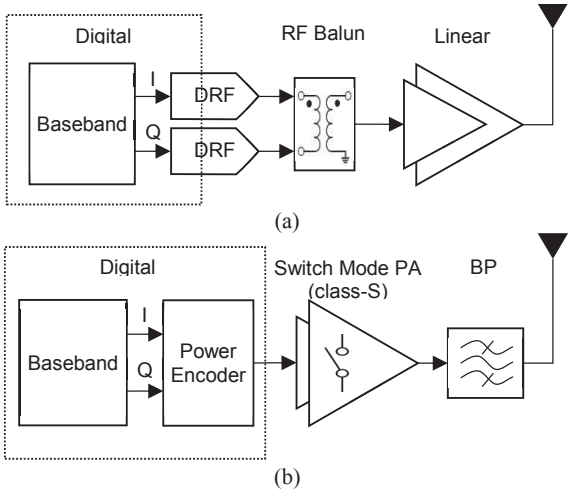

Fig. 1. Two digital-RF transmitter architectures based on (a) linear PA, and (b) switch mode PA, respectively.

However, the very low power coding efficiency (<30%) of the traditional power encoders (delta sigma modulator (DSM) [2], noise shaped pulse width modulator (PWM) [3], [4] and pulse position modulator (PPM) [5]) cause total TX efficiency degradation. It becomes even worse for signals with high PAPR (peak-to-average power ratio)>8dB, like LTE signal. To address this challenge, our group recently proposed a new multi-level intermediate frequency pulse width modulation (ML-IFPWM) with key features of high power coding efficiency, linearization and less hardware demand, as reported in [6].

In this work, we will focus on the practical implementation and demonstration of an All-Digital GHz transmitter using a commercially available FPGA (Field Programmable Gate Array) board with the proposed efficient ML-IFPWM concept. To our knowledge, this is the first implemented real-time discrete-time (DT) domain multi-level PWM coding approach for a 2-GHz digital transmitter using LTE signal achieving power coding efficiency higher than 45%. The paper is organized as follows: Section II will review the proposed multi-level IF PWM power coding scheme for class-S PA, and Section III will the FPGA implementation in details. The measurement results are discussed in Section IV, with a conclusion at the end.

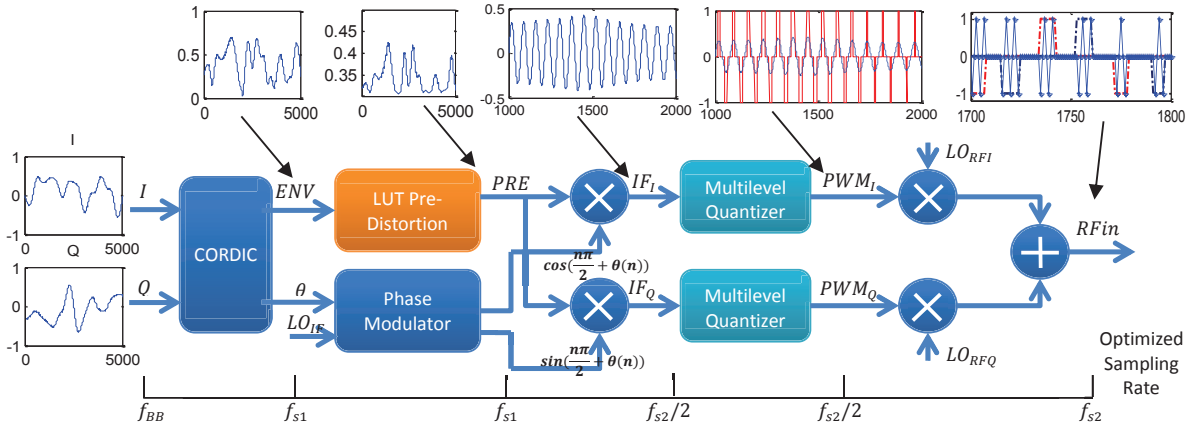

Fig. 2. ML-IFPWM power coding diagram.

II. ML-IFPWM Power Coding Algorithm

To achieve the high power coding efficiency, a ML-IFPWM power coding algorithm combing look-up table (LUT) pre-distortion is developed [6]. As illustrated in Fig. 2, ML-IFPWM is realized by decreasing the PWM encoder operation frequency from (several tens of GHz in RFPWM) to an IF of MHz (e.g., $LO_{IF} = 61.44$ MHz), and then performing the power encoding with Cartesian IQ signals by two multi-level quantizers. The generated PWM_I and PWM_Q with the minimized bit-resolution are digitally up-converted to RF using the 4-phase LO_{RF}, see (1)

$$RF_{in} = PWM_I \cdot LO_{RFI} + PWM_Q \cdot LO_{RFQ} \quad (1)$$

where $LO_{RFI}(m) = \cos\left(2\pi\frac{f_{s2}}{4}\frac{m}{f_{s2}}\right) = \{\dots 1,\ 0, -1, 0, \dots\}$,

$LO_{RFQ}(m) = \sin\left(2\pi\frac{f_{s2}}{4}\frac{m}{f_{s2}}\right) = \{\dots 0, 1, 0, -1, \dots\}$, $m \in N$

The LUT pre-distortion for correction the nonlinearity introduced by the power encoder based on the derived AM-AM transfer function of the multi-level quantizers:

$$f(a(t)) = \frac{1}{N}\sum_{i=1}^{N}\cos\left[\sin^{-1}\left(\frac{V_{thi}}{a(t)}\right)\right],\ a(t) \geq V_{thN} \quad (2)$$

where $a(t)$ is the envelope, and V_{thi} is the i^{th} threshold value, $V_{thi} < V_{thj}$ when $1 \leq i < j \leq N$. Therefore, the inverse function of (2) could be numerically solved by building a look-up table mapping ($PRE = LUT(ENV)$). The LUT pre-distorts the envelope information. The original phase information is converted back by (3), (4) using an IF carrier LO_{IF}, here choose $LO_{IF} = \frac{f_{s1}}{4}$.

$$IF_I(n) = PRE(n) \cdot \cos(2\pi\frac{f_{s1}}{4}\frac{n}{f_{s1}} + \theta(n)) \quad (3)$$

$$IF_Q(n) = PRE(n) \cdot \sin(2\pi\frac{f_{s1}}{4}\frac{n}{f_{s1}} + \theta(n)) \quad (4)$$

where PRE and θ are the pre-distorted envelope and the phase of the IQ signals, respectively. The sampling rate of each stage is also optimized to ensure the required resolution for signal processing, as labeled on Fig. 2.

In order to evaluate the performance of this ML-IFPWM algorithm, a co-simulation bench is built in Agilent SystemVue and MATLAB. As illustrated in Fig.3, the real test signal is generated from SystemVue LTE library, and then processed by MATLAB. The results are fed back to SystemVue to check the EVM.

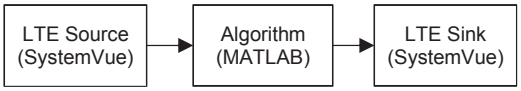

Fig. 3. SystemVue-MATLAB Co-Simulation Bench.

Using the 3-level IFPWM encoder, for 5-MHz 9.85dB PAR LTE signal, 46.26% power coding efficiency and 5.45% EVM are achieved, for 20-MHz 10.25dB PAR LTE signal, 38.66% power coding efficiency and 5.87% EVM are also obtained in simulation [6].

III. FPGA Implementation

So far, the published power coding algorithms are mainly theoretically evaluated in the simulation like [4]. Very few works are reported regarding their practical implementation, in specifics with the real-time discrete-time domain using commercial signal processor chips. This is mainly due to the extremely high oversampling clock (several tens of GHz) requirement in the power coding algorithms, which exerts big challenges on the GHz digital TX implementation. Off-line implementation [2] is employed for testing purpose using AWG (arbitrary waveform generator). With the rapid development of signal processor technology, commercial available FGPA is getting preferred in the SDR due to its re-configurability. Next part, we will describe in details the procedure of IF-MLPWM FPGA implementations.

A. Challenges and Solutions

Sampling rate challenge: High output sampling rate is essential to faithfully quantize multi-level IF signals and generate the GHz digital-RF bits. In order to achieve such high throughput, the high speed part must be implemented in parallel. A carefully designed polyphase interpolation filter forwards the same input to the paralleled units, each

unit maintains the low sampling rate. After encoding the IF, the paralleled outputs sequentially transmit out through on-chip GTX, a FPGA parallel-to-serial (P/S) converter.

Channel-to-channel phase alignment challenge: Ideally, multiple channels operate synchronously for sending out the control bits signal. However, variable clock skews of GTX channels due to the slightly difference of routed paths length will affect the phase alignment of multiple channel outputs. Therefore, the phase alignment has to been considered to perform the channel-to-channel de-skew. By aligning multiple GTX transmitters to a common clock, the only phase difference is the skew from the common clock, and all channels transmit data simultaneously as long as the path latency is matched.

B. System Architecture

ML-IFPWM is a multi-rate discrete time (DT) system. According to the LTE standard, the baseband sample rates (f_{BB}) are 15.36 MSps and 61.44 MSps for 5-MHz and 20-MHz bandwidth, respectively. The first stage sampling rate (f_{s1}), which also equals to the system clock frequency, is related to the FPGA specification. But the actual maximum frequency depends on the design complexity. To reach FPGA timing closure in this design f_{s1} is estimated to be less than 300 MSps from simulation. Therefore, choose $f_{s1} = 4 \times LO_{IF} = 245.7$ MSps , that equals an up-sampling ratio of 16 or 4 to the 5-/20-MHz bandwidth baseband signal. In addition, choose the final stage sample rate $f_{s2} = 7864.32$ MSps, an up-sampling ratio of 32 to the first stage, for:

$$LO_{RF} = \frac{f_{s2}}{4} = 1966.08 \text{ MHz}.$$

With the above assigned sampling rates, the whole system architecture could be deployed. A digital-RF transmitter employing 3-level IFPWM is illustrated in Fig. 4, including digital pre-distortion, power encoder, Parallel to Series converter, buffer driver, SMPA and bandpass filter. In this prototype, a 3-level IFPWM power encoder for 5-MHz bandwidth LTE input is employed with Xilinx VC-707 board.

C. Block Description

The main blocks in design are explained as follows:

1). Digital Pre-Distortion

As shown in Fig. 5, the digital pre-distortion block consists of a CORDIC (coordinate rotation digital computer), an interpolator, two scalars, a block ROM LUT, a DDS (direct digital synthesis) and two multipliers. First of all, the CORDIC will split the amplitude and the phase information from the baseband Cartesian IQ inputs. Then the interpolator, which is built by an up-sampler performing zero padding and a FIR filter removing the spectral replicas, increases the sampling rate from 15.36 MSps to 245.7 MSps by a ratio of 16. Next, two scalars are carefully designed to map the interpolated magnitude and phase signal into the 10-bits ROM integer address range [0 2^{10}-1] and the pre-defined DDS phase input range [-0.5 0.5], respectively. The LUT mapping matrix is stored in the block ROM, which is the inverse function of (2) when i=1 for 3-level IFPWM. And the DDS (direct digital synthesizer) streams the original phase to modulate a 61.44 MHz IF carrier. It will generate two 90º out-of-phase signals. Finally, two multipliers multiply these signals with the pre-distorted envelope to reconstruct the IF_I and IF_Q in (3) and (4).

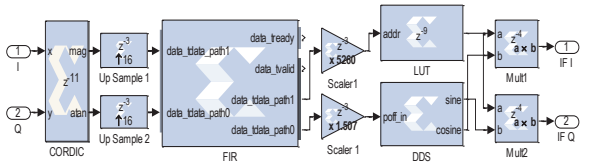

Fig. 5. Digital pre-distortion block diagram.

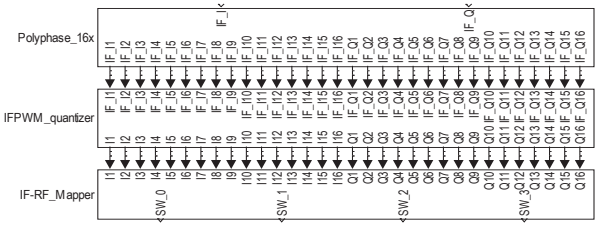

Fig. 6. Power encoder block diagram.

2). Power Encoder:

Power encoder is the core block. As shown is Fig. 6, it includes a set of polyphase interpolation filter bank, IFPWM quantizers, digital IF-RF converters and mappers. The polyphase filter bank divides the phase by 16 paralleled units for both I and Q paths, in which the calculated coefficients are assigned for associated FIR taps. Then, each unit connects a memory-less IFPWM quantizer. After that, the IF IQ signals are converted to

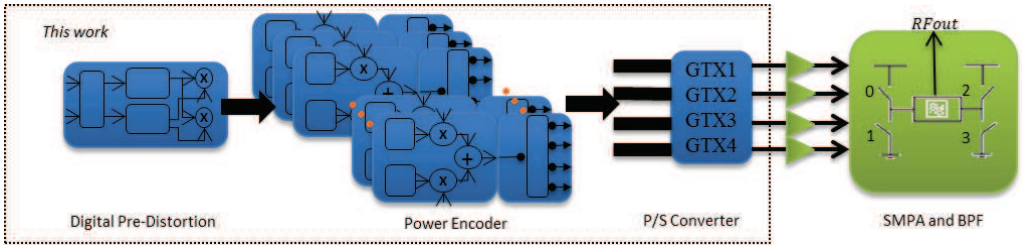

Fig. 4. System architecture diagram of All-Digital transmitter with FPGA implemented front end.

3-level IFPWM waveforms by comparing the amplitude with the fixed thresholds [6]. As mentioned above, this process needs sufficient time resolution to achieve a decent SNDR (signal-to-noise-distortion-ratio), therefore the sampling rate as high as $\frac{f_{S2}}{2} = 3932.16$ MSps is optimized from simulation, which also determines the number of paralleled units ($\frac{3932.16}{245.76} = 16$). Next, the digital IF-RF converter mixes carrier frequency to RF according to (1). The resulted RF signal is a 3-level PWM, 32 divided phase in parallel. Eventually, the mapper further splits 3-level PWM to four 32-bits binary outputs. The mapping algorithm is presented in [6].

3). P/S converter:

The P/S converter consists of a user clock source, a phase alignment module, four start-up FSMs (finite state machine), and four GTXs. The user clock source buffers the external differential precise clocks from SMA pins to provide the reference clock to GTXs. It also buffers the TXOUTCLK from the master GTX as the common clock for phase alignment, which is performed by the phase alignment module after resetting or powering up the GTX. That module sends PHALIGNMENT_DONE signal to four start-up FSMs to synchronize all related GTXs when lane-to-lane de-skew requirement is met. Finally, four critical GTXs each serializes the 32-bits signal to 1-bit with 32x faster speed. That is achieved with its built in quad PLL.

IV. Measurement Results

The baseband test signal, 15360 points of 5-MHz 9.85dB PAR LTE signal, is also compiled in the FPGA ROM. 20-GSps LeCory high speed oscilloscope probes 4 channel switching signals and calculate the 3-Level switching waveform using its built-in Math function, see Fig. 7. In addition, the measured 3-level IFPWM output spectrum is given in Fig. 8. The RF is centered at 1.904GHz for LTE band-2. The SNDR is more than 35dB, and the calculated coding efficiency is 46.13%. The measured performance is in good aggrement with the simulated ones, which confirm the successful implementation of the power encoder in FPGA.

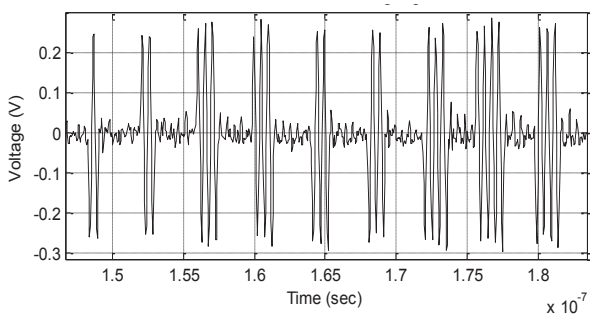

Fig. 7. Measured 3-Level final output from power encoder .

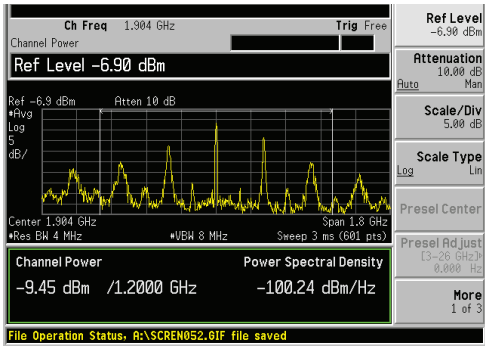

Fig. 8. Measured spectrum from output of power encoder. .

V. Conclusion

A FPGA implementable GHz digital TX architecture has been show. High speed digital bits from multi-level IF pulse width modulator for class-S PA at 1.9-GHz LTE signals has been demonstrated in this work with record power coding efficiency. The generated platform offers a variety of potential advantages, including configurability, and easy integration into baseband SoC. The use of this power encoding eliminates the need for many high speed analog/RF components, and enables the use of high efficiency class-S PA in digital base station. Future work on wider bandwidth using higher level will be conducted.

Acknowledgement

The authors wish to thank A. Knyazev, T. Koike-Akino, P. Orlik, and K. Parsons in Mitsubishi Electric Research Labs, for the valuable discussions.

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